DS481 Low Power RS-485/RS-422 Multipoint Transceiver with Sleep Mode

Check for Samples: DS481

FEATURES

- **Meets TIA/EIA RS-485 Multipoint Standard**
- **Sleep Mode Reduces I_{CC} to 0.2 µA**
- **Guaranteed Full Load Output Voltage (V_{OD3})**
- **Low Quiescent Current: 200 µA typ**
- **−7V to +12V Common-mode Input Voltage Range**
- **TRI-STATE Outputs on Driver and Receiver**
- **AC Performance:**
  - **Driver Transition Time: 25 ns typ**
  - **Driver Propagation Delay: 40 ns typ**
  - **Driver Skew: 1 ns typ**
  - **Receiver Propagation Delay: 200 ns typ**
  - **Receiver Skew: 20 ns typ**
- **Half-duplex Flow Through Pinout**
- **Operates From a Single 5V Supply**
- **Allows up to 64 Transceivers on the Bus**
- **Current-limiting and Thermal Shutdown for Driver Overload Protection**
- **Industrial Temperature Range Operation**
- **Pin and Functional Compatible with MAX481C and MAX481E**

DESCRIPTION

The DS481 is a low-power transceiver for RS-485 and RS-422 communication. The device contains one driver and one receiver. The drivers slew rate allows for operation up to 2.0 Mbps (see Applications Information).

The transceiver draws 200 µA of supply current when unloaded or 0.2 µA when in the automatic sleep mode. Sleep mode is activated by inactivity on the enables (DE and RE(1)). Holding DE =L and RE(1) =H for greater than 600 ns will enable the sleep mode. The DS481 operates from a single +5V supply.

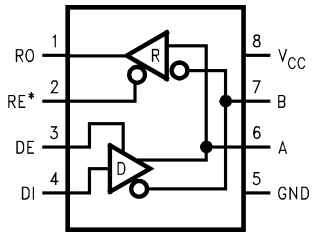
The driver is short-circuit current limited and is protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into TRI-STATE (High Impedance state) under fault conditions. The driver guarantees a minimum of 1.5V differential output voltage with maximum loading across the common mode range (V_{OD3}).

The receiver has a failsafe feature that guarantees a logic-high output if the input is open circuit.

The DS481 is available in a surface mount package and is characterized for Industrial temperature range operation.

(1) Non Terminated, Open Input only

Connection and Logic Diagram



*Non Terminated, Open Input only

Figure 1. SOIC Package

Table 1. Pin Descriptions

Pin Name	Number	DESCRIPTION
RO	1	Receiver Output: When RE (Receiver Enable) is LOW, the receiver is enabled (ON), if DO/RI ≥ DO (1)/RI (1) by 200 mV, RO will be HIGH. If DO/RI ≤ DO (1)/RI (1) by 200 mV, RO will be LOW. Additionally RO will be HIGH for OPEN (Non-terminated) Inputs.
RE (1)	2	Receiver Output Enable: When RE (1) is LOW the receiver output is enabled. When RE (1) is HIGH, the receiver output is in TRI-STATE (OFF). When RE (1) is HIGH and DE is LOW, the device will enter a low-current sleep mode after 600 ns.
DE	3	Driver Output Enable: When DE is HIGH, the driver outputs are enabled. When DE is LOW, the driver outputs are in TRI-STATE (OFF). When RE (1) is HIGH and DE is LOW, the device will enter a low-current sleep mode after 600 ns.
DI	4	Driver Input: When DE (Driver Enable) is HIGH, the driver is enabled, if DI is LOW, then DO/RI will be LOW and DO (1)/RI (1) will be HIGH. If DI is HIGH, then DO/RI is HIGH and DO (1)/RI (1) is LOW.
GND	5	Ground Connection.
DO/RI	6	Driver Output/Receiver Input, 485 Bus Pin.
DO (1) /RI (1)	7	Driver Output/Receiver Input, 485 Bus Pin.
V_{CC}	8	Positive Power Supply Connection: Recommended operating range for V_{CC} is +4.75V to +5.25V.

(1) Non Terminated, Open Input only

Truth Table

DRIVER SECTION				
RE (1)	**DE**	**DI**	**A**	**B**
X(2)	H	H	H	L
X(2)	H	L	L	H
X(2)	L	X(2)	Z(2)	Z(2) (3)
RECEIVER SECTION				
RE (1)	**DE**	**A-B**		**RO**
L	L	≥+0.2V		H
L	L	≤−0.2V		L
H	X(2)	X(2)		Z (2)(3)
L	L	OPEN (1)		H

(1) Non Terminated, Open Input only
(2) X = indeterminate
Z = TRI-STATE
(3) Device enters sleep mode if enable conditions are held > 600 ns, DE = L and RE = H. RE is Non Terminated and Open Input only.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage (V_{CC})	+12V
Enable Input Voltage (RE (3), DE)	−0.5V to (V_{CC} + 0.5V)
Driver Input Voltage (DI)	−0.5V to (V_{CC} + 0.5V)
Driver Output Voltage (A, B)	−14V to +14V
Receiver Input Voltage (A, B)	−14V to +14V
Receiver Output Voltage (RO)	−0.5V to (V_{CC} + 0.5V)
Maximum Package Power Dissipation @ +25°C	
D0008A Package	1.19W
Derate D0008A Package 9.5 mW/°C above +25°C	
Maximum Package Power Dissipation @ +70°C	
D0008A Package	0.76W
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
(Soldering, 4 sec.)	+260°C
ESD (HBM)	≥2 kV

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Non Terminated, Open Input only

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Operating Free Air				
Temperature (T_A)				
DS481T	−40	+25	+85	°C
Bus Common Mode Voltage	−7		+12	V

Electrical Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified (1) (2)

Parameter		Test Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage	(No Load)	A, B	1.5		5	V
V_{OD2}	Differential Driver Output Voltage with Load	R_L = 50Ω, (RS422), Figure 2		2	2.8		V
		R_L = 27Ω, (RS485), Figure 2		1.5	2.3	5	V
ΔV_{OD}	Change in Magnitude of Output Differential Voltage	R_L = 27Ω or 50Ω (3)				0.2	|V|
V_{OD3}	Differential Driver Output Voltage—Full Load with Max V_{CM}	R1 = 54Ω, R2 = 375Ω V_{TEST} = −7V to +12V, Figure 3		1.5	2.0	5	V
V_{OC}	Driver Common-Mode Output Voltage	R_L = 27Ω or 50Ω, Figure 2		0		3	V
ΔV_{OC}	Change in Magnitude of Common-Mode Output Voltage	R_L = 27Ω or 50Ω, Figure 2 (3)				0.2	|V|

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except $V_{OD1/2/3}$ and V_{ID}.
(2) All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input changes state.

Electrical Characteristics (continued)

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified (1) (2)

Parameter		Test Conditions		Pin	Min	Typ	Max	Units
V_{IH}	Input High Voltage			DI, DE, RE (4)	2.0			V
V_{IL}	Input Low Voltage						0.8	V
I_{IN1}	Input Current	V_{IN} = 0V or V_{CC}					±2	µA
I_{IN2}	Input Current (5) DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = +12V	DS481T	A, B	0	190	500	µA
		V_{IN} = −7V			0	−100	−400	µA
V_{TH}	Receiver Differential Threshold Voltage	−7V ≤ V_{CM} ≤ +12V			−0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V				70		mV
V_{OH}	Receiver Output High Voltage	I_O = −4 mA, V_{ID} = 0.2V		RO	3.5			V
V_{OL}	Receiver Output Low Voltage	I_O = 4 mA, V_{ID} = −0.2V					0.5	V
I_{OZR}	TRI-STATE Output Current at Receiver	0.4V ≤ V_O ≤ 2.4V					±1	µA
R_{IN}	Receiver Input Resistance	−7V ≤ V_{IN} ≤ +12V	DS481T	A, B	24			kΩ
I_{CC}	No-Load Supply Current (6)	DE = V_{CC}, RE (4) = 0V or V_{CC}		V_{CC}		200	500	µA
		DE = 0V, RE (4) = 0V or V_{CC}				200	500	µA
I_{CCX}	Sleep Mode Supply Current	DE = GND RE (4) = V_{CC} (Figure 15)		V_{CC}		0.2	10	µA
I_{OSD1}	Driver Short Circuit Current, V_O = HIGH	−7V ≤ V_O ≤ +12V		A, B			250	mA
I_{OSD2}	Driver Short Circuit Current, V_O = LOW	−7V ≤ V_O ≤ +12V					−250	mA
I_{OSR}	Receiver Short Circuit Current	V_O = GND		RO	7		85	mA

(4) Non Terminated, Open Input only.
(5) I_{IN2} includes the receiver input current and driver TRI-STATE leakage current.
(6) Supply current specification is valid for loaded transmitters when DE = 0V or enabled (DE = H) with no load.

Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified (1) (2) (3)

Parameter		Test Conditions	Min	Typ	Max	Units
t_{PLHD}	Driver Differential Propagation Delay—Low to High	R_L = 54Ω, C_L = 100 pF	10	40	80	ns
t_{PHLD}	Driver Differential Propagation Delay—High to Low		10	39	80	ns
t_{SKEW}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	1	10	ns
t_r	Driver Rise Time		3	25	50	ns
t_f	Driver Fall Time		3	25	50	ns
t_{ZH}	Driver Enable to Output High	C_L = 100 pF		50	200	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100 pF		65	200	ns
t_{LZ}	Driver Disable from Output Low	C_L = 15 pF		80	200	ns
t_{HZ}	Driver Disable from Output High	C_L = 15 pF		80	200	ns
t_{PSH}	Driver Enable from Sleep Mode to Output High	C_L = 100 pF (4)(Figure 6, Figure 7)	70	98	250	ns
t_{PSL}	Driver Enable from Sleep Mode to Output Low	C_L = 100 pF (4)(Figure 8 ,Figure 9)	70	98	250	ns
t_{PLHD}	Receiver Differential Propagation Delay—Low to High	C_L = 15 pF (RO)	30	190	400	ns
t_{PHLD}	Receiver Differential Propagation Delay—High to Low		30	210	400	ns
t_{SKEW}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	20	50	ns
t_{ZH}	Receiver Enable to Output High	C_L = 15 pF		45	150	ns
t_{ZL}	Receiver Enable to Output Low			40	150	ns
t_{LZ}	Receiver Disable from Output Low			50	150	ns
t_{HZ}	Receiver Disable from Output High			55	150	ns
t_{PSH}	Receiver Enable from Sleep Mode to Output High	C_L = 15 pF (4)(Figure 12, Figure 14)	70	97	250	ns
t_{PSL}	Receiver Enable from Sleep Mode to Output Low	C_L = 15 pF (4)(Figure 12, Figure 13)	70	95	250	ns
t_{SLEEP}	Time to Sleep (Device)	DE = L and RE (5) = H (Figure 15)	50		600	ns
f_{max}	Maximum Data Rate	(6)	2.0			Mbps

(1) All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.
(2) f = 1 MHz, t_r and t_f ≤ 6 ns, Z_O = 50Ω.
(3) C_L includes jig and probe capacitance.
(4) For enable from sleep mode delays DE = L and RE = H for greater than 600 ns prior to test (device is in sleep mode). RE is Non Terminated, Open Input only.
(5) Non Terminated, Open Input only
(6) f_{max} is the guaranteed data rate for 50 ft of twisted pair cable. f_{max} may be conservatively determined from the ratio of driver transition time (t_r) to the data rate unit interval ($1/f_{max}$). Using a 10% ratio yields f_{max} = (0.1)/50 ns = 2.0 Mb/s. Higher data rates may be supported by allowing larger ratios.

PARAMETER MEASUREMENT INFORMATION

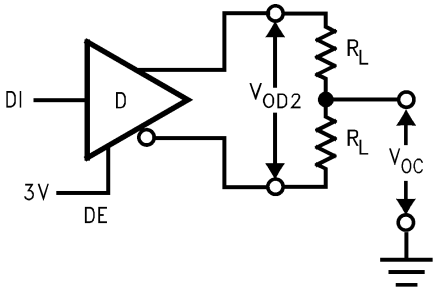


Figure 2. V_{OD}

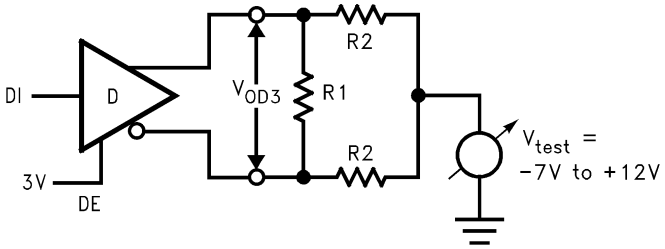


Figure 3. V_{OD3}

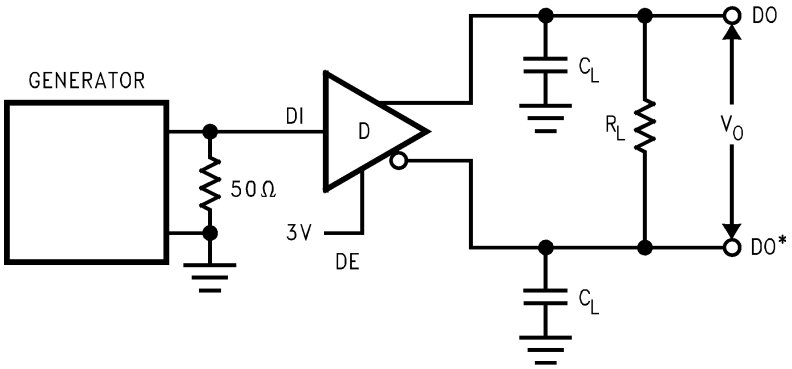


Figure 4.

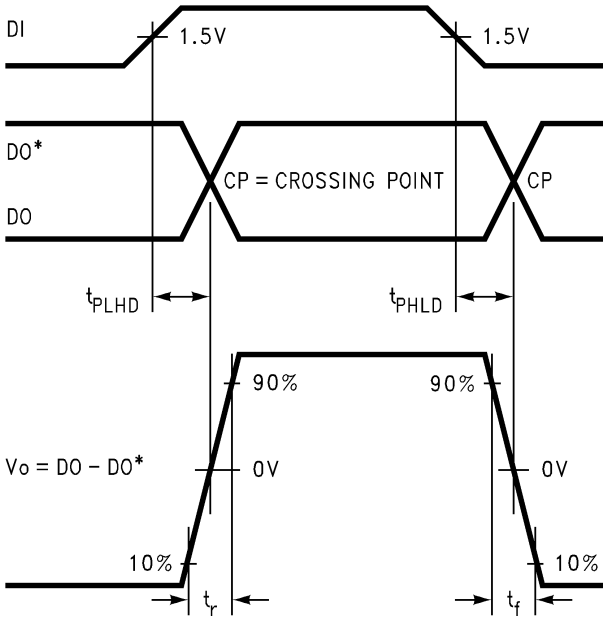


Figure 5.

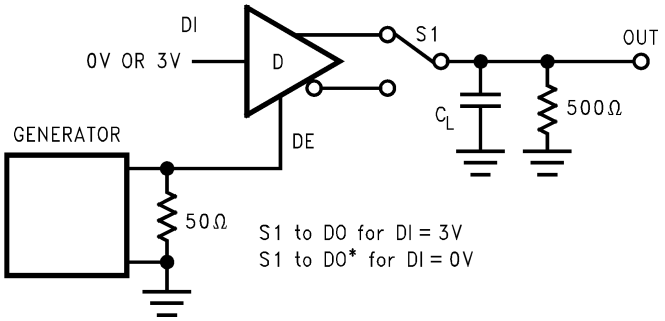


Figure 6.

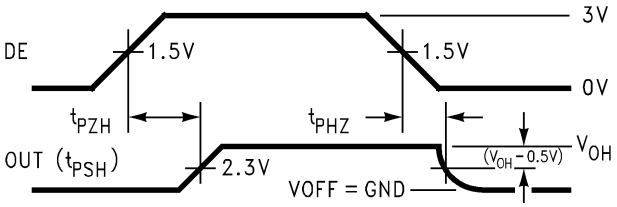


Figure 7.

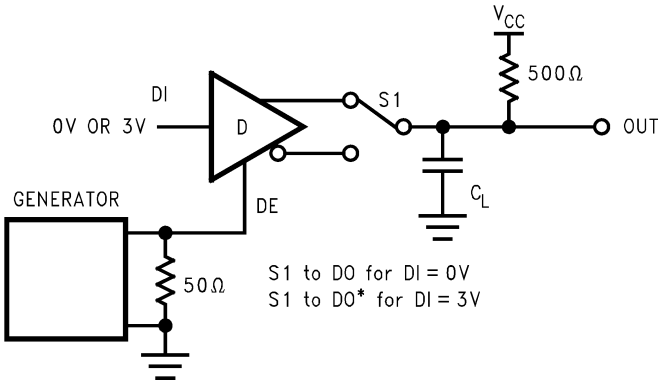


Figure 8.

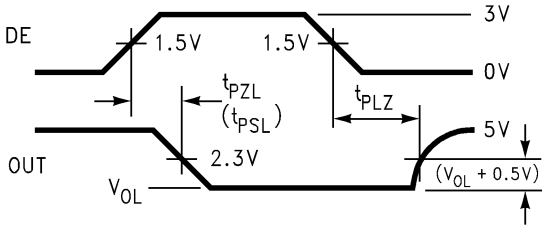


Figure 9.

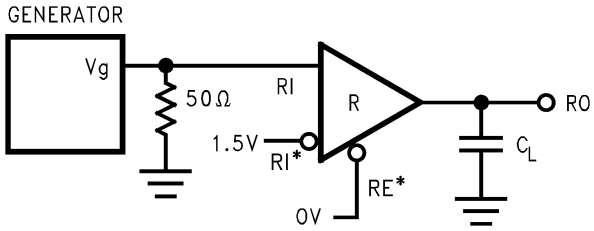


Figure 10.

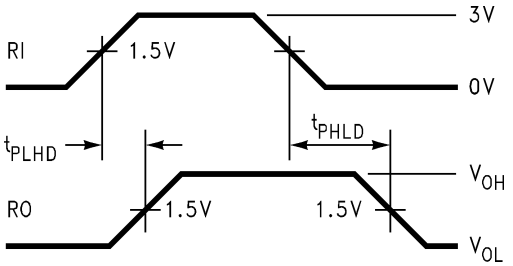


Figure 11.

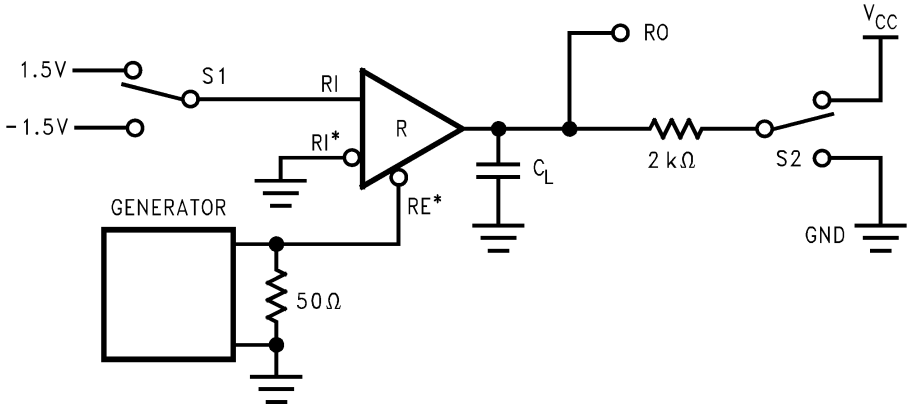


Figure 12.

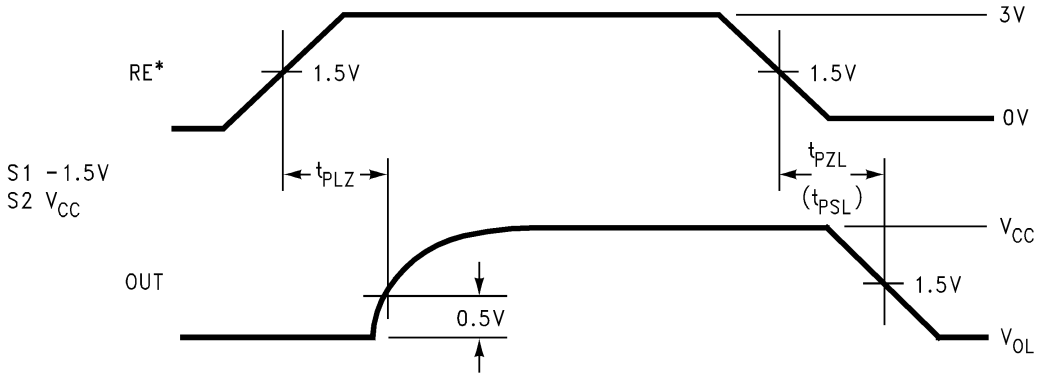


Figure 13.

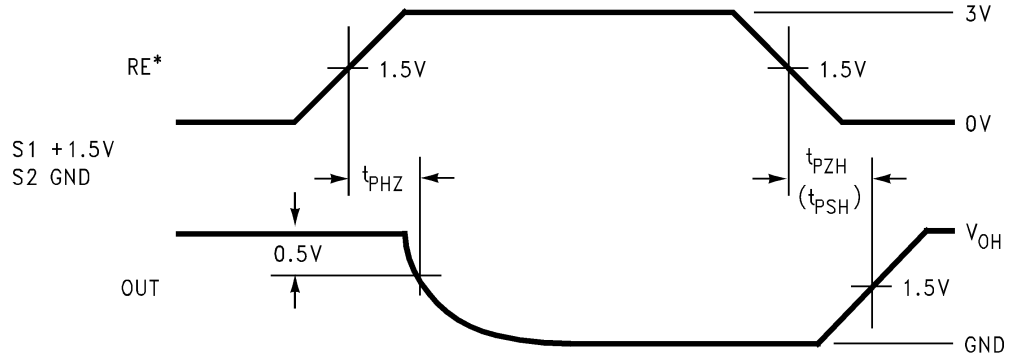
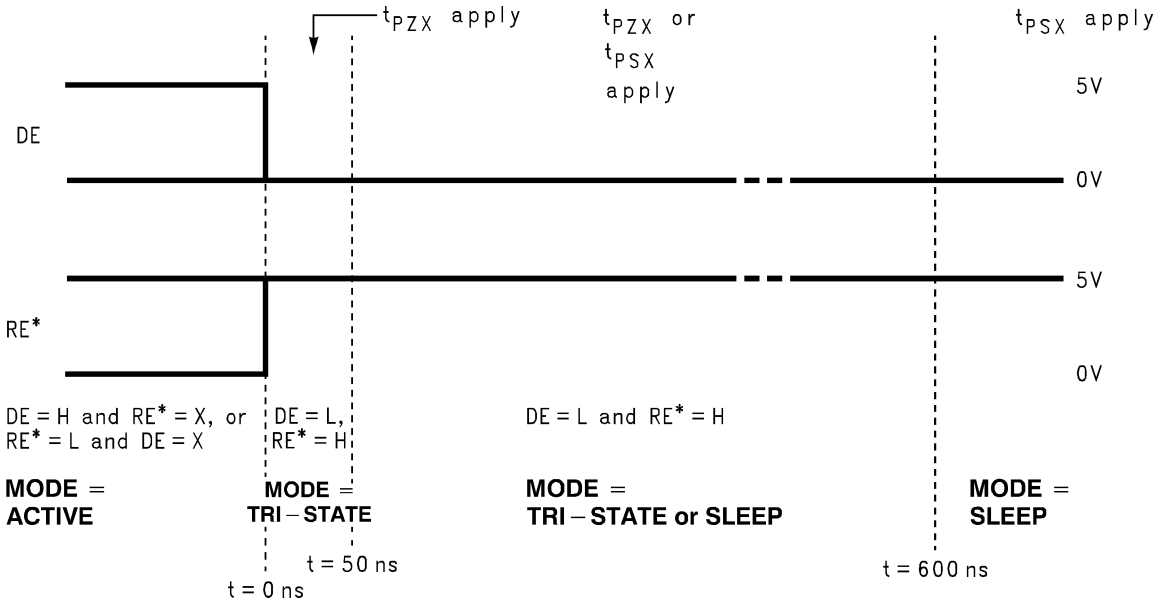


Figure 14.



*Note: Non Terminated, Open Input only

Figure 15. Entering Sleep Mode Conditions (modes and exit parameters shown)

Unit Load

A unit load for an RS-485 receiver is defined by the input current versus the input voltage curve. The gray shaded region is the defined operating range from −7V to +12V. The top border extending from −3V at 0 mA to +12V at +1 mA is defined as one unit load. Likewise, the bottom border extending from +5V at 0 mA to −7V at −0.8 mA is also defined as one unit load (see Figure 16). An RS-485 driver is capable of driving up to 32 unit loads. This allows up to 32 nodes on a single bus. Although sufficient for many applications, it is sometimes desirable to have even more nodes.

The DS481 has ½ unit load and will allow up to 64 nodes guaranteed over temperature.

For a ½ UL device the top and bottom borders shown in Figure 16 are scaled. Both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.5 mA for the top border and −7V at −0.4 mA for the bottom border (see Figure 16). Again, both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.25 mA for the top border and −7V at −0.2 mA for the bottom border (see Figure 16).

The advantage of the ½ UL device is the increased number of nodes on one bus. In a single master multi-slave type of application where the number of slaves exceeds 32, the DS481 may save in the cost of extra devices like repeaters, extra media like cable, and/or extra components like resistors.

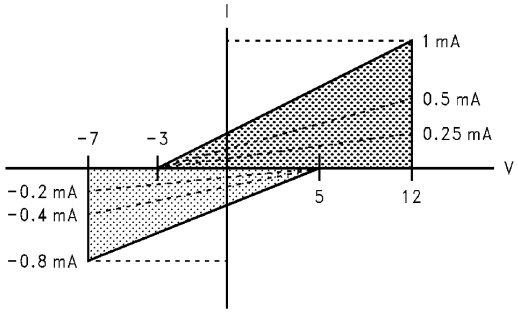


Figure 16. Input Current vs Input Voltage Operating Range

Sleep Mode

The DS481 features an automatic sleep mode that allows the device to save power when not transmitting data. Since the sleep mode is automatic, no external components are required. It may be used as little or as much as the application requires. The more the feature is utilized, the more power it saves.

The sleep mode is automatically entered when both the driver and receiver are disabled. This occurs when both the DE pin is asserted to a logic low and the $\overline{RE}$(7) pin is asserted to a logic high. Once both pins are asserted the device will enter sleep mode after 50 ns. The DS481 is guaranteed to go into sleep mode within 600 ns after both pins are asserted. The device wakes up (comes out of sleep mode) when either the DE pin is asserted to a logic high and/or the $\overline{RE}$(7) pin is asserted to a logic low. After the device enters sleep mode it will take longer for the device to wake up than it does for the device to enable from TRI-STATE. Refer to datasheet specifications t_{PSL} and t_{PSH} and compare with t_{PZL} and t_{PZH} for timing differences.

The benefit of the DS481 is definitely its power savings. When active the device has a maximum I_{CC} of 500 µA. When in sleep mode the device has a maximum I_{CC} of only 10 µA, which is 50 times less power than when active. The I_{CC} when the device is active is already very low but when in sleep mode the $I_{CC}$is ultra low.

(7) Non Terminated, Open Input only

APPLICATIONS INFORMATION

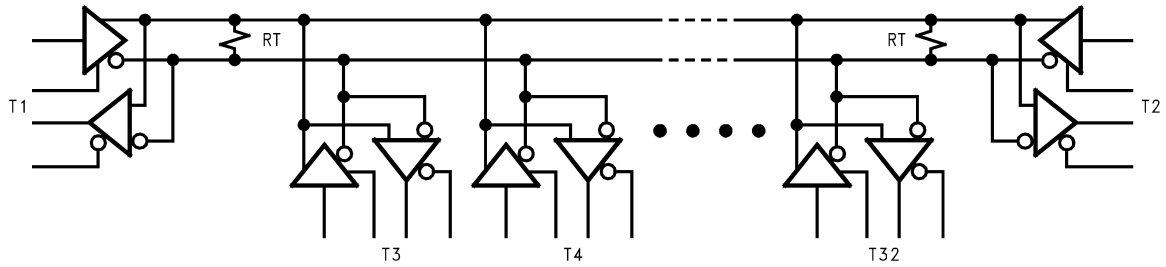


Figure 17. Multipoint RS-485 Application

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS481TM/NOPB	LIFEBUY	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS481 TM	
DS481TMX/NOPB	LIFEBUY	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS481 TM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

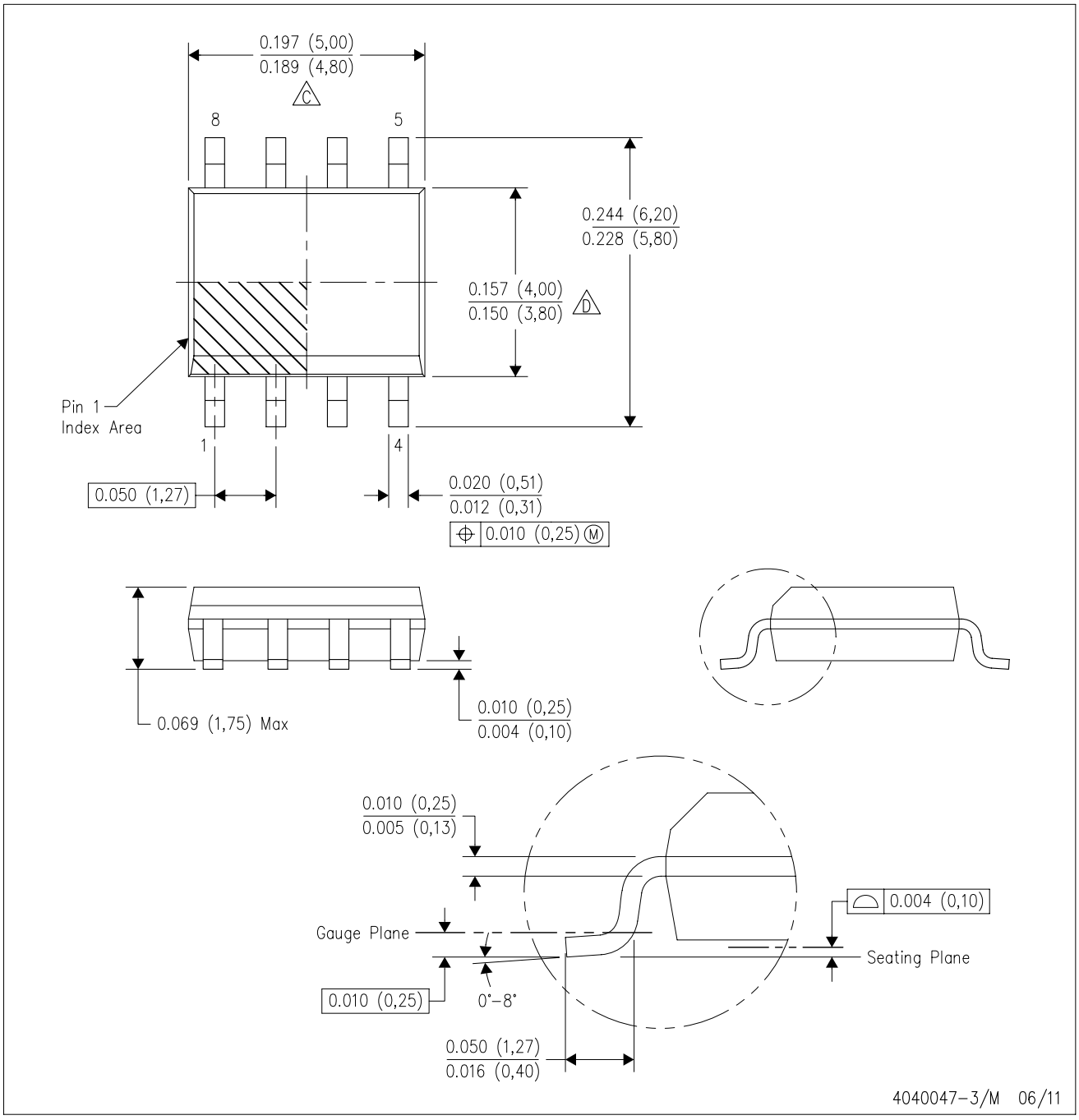
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265